considered.

IN THE SPECIFICATION

No amendments to the specification are submitted.

IN THE DRAWINGS

No amendments to the drawings are submitted, therefore, please use the drawings presented within the reissue application which are copied from the issued patent.

IN THE CLAIMS

Please add the claims as follows.

21. A method of controlling an integrated regulator circuit used in a power conversion system, comprising:

controlling a switching signal of the integrated regulator circuit in response to a feedback signal; and

receiving a state control signal external from the integrated regulator circuit to set a mode of operation of the regulator circuit.

22. The method of claim 21 wherein the state control signal allows the switching signal of the integrated regulator circuit to switch over multiple cycles during a first mode of operation.

23. The method of claim 22 wherein the state control signal disables the integrated regulator circuit in a second mode of operation.

24. The method of claim 23 wherein the state control signal disables the integrated regulator circuit for multiple cycles of the switching signal.

25. The method of claim 21 further including:

comparing the state control signal to a reference signal and generating a mode signal; and

setting the mode of operation of the integrated regulator circuit according to the mode signal.

26. The method of claim 21 further including storing the mode signal in a memory circuit to set the mode of operation of the integrated regulator circuit.

27. A method of controlling an integrated regulator circuit in a power converter, comprising:

controlling a switching signal of the integrated regulator circuit in response to a feedback signal; and

providing a control signal to the integrated regulator circuit which alters the switching signal of the integrated regulator circuit over multiple cycles of the switching signal.

28. The method of claim 27 wherein the control signal alters the output signal of the integrated regulator circuit to disable the power converter.

29. The method of claim 27 wherein the state control signal alters the output signal of the integrated regulator circuit to reduce power conversion of the power converter.

30. The method of claim 27 further including:

comparing the control signal to a reference signal and generating a mode signal; and

setting a mode of operation of the integrated regulator circuit according to the mode signal to alter the output signal of the regulator circuit.

31. The method of claim 30 further including storing the mode signal in a memory circuit to set the mode of operation of the integrated regulator circuit.

32. An integrated circuit containing a regulator circuit, the regulator circuit comprising:

a control circuit having an input coupled for receiving a control signal from external to the regulator circuit and an output for providing a mode signal in response to the control signal; and

a switching regulator circuit having a first input coupled for receiving a feedback signal, an output for providing a switching signal of the regulator circuit, and a control input coupled for receiving the mode signal to set a mode of operation of the switching regulator circuit.

33. The regulator circuit of claim 32, wherein the control circuit includes a comparator having a first input coupled for receiving a control signal, a second input coupled for receiving a first reference signal, and an output for providing the mode signal.

34. The regulator circuit of claim 33, wherein the control circuit further includes a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit as the mode signal according to a value of the control signal.

35. The regulator circuit of claim 34, wherein the memory circuit has at least one storage element for storing the mode of operation of the regulator circuit.

36. The regulator circuit of claim 34, wherein the control circuit further includes a resistor divider network for generating the first reference signal at a first output and the second reference signal at a second output.

37. The regulator circuit of claim 33, wherein the comparator includes:

a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

38. A semiconductor chip having at least three external connections, comprising:

a switching regulator operating in response to a feedback signal for providing a switching signal;

a first terminal for providing the switching signal from the switching regulator;

a second terminal coupled for receiving the feedback signal; and

a third terminal coupled for receiving a control signal which sets a mode of operation of the switching regulator.

39. The semiconductor chip of claim 38 further including a state circuit having an input coupled for receiving the state control signal and having an output coupled to a control input of the switching regulator.

40. The semiconductor chip of claim 39, further comprising a fourth electrical connection terminal for coupling an external ground reference to an internal ground reference of the switching regulator.

41. In a power conversion system, an integrated switching regulator circuit operating in response to a feedback signal from the power conversion system for providing a switching signal to the power conversion system, the integrated switching regulator comprising a control input coupled for receiving an operating mode control signal from external to the switching regulator circuit which sets a mode of operation of the switching regulator circuit.

42. The integrated switching regulator circuit of claim 41 further including a state control circuit having an input coupled for receiving the operating mode control signal and an output for providing a mode signal in response to the state control signal to set the mode of operation of the switching regulator circuit.

43. The integrated switching regulator circuit of claim 42, wherein the state control circuit includes a comparator having a first input coupled for receiving the operating mode control signal, a second input coupled for receiving a first reference signal, and an output for providing the mode signal.

44. The integrated switching regulator circuit of claim 43, wherein the state control circuit further includes a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit as the mode signal according to a value of the control signal.

45. An integrated regulator circuit providing a drive signal used to regulate power transfer of a power supply in response to a feedback signal and receiving an external control signal used to suspend power transfer of the power supply, the integrated regulator circuit comprising:

a control circuit having an input coupled for receiving the external control signal and an output for providing a mode signal in response to the external control signal; and

a switching regulator circuit having a first input coupled for receiving the feedback signal, a control input coupled for receiving the mode signal, and an output for providing a switching signal in response to the feedback signal and the mode signal.

46. The integrated regulator circuit of claim 45, wherein the control circuit includes a comparator having a first input coupled for receiving a control signal, a second input coupled for receiving a first reference signal, and an output for providing the mode signal.

47. The integrated regulator circuit of claim 46, wherein the control circuit further includes a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit as the mode signal according to a value of the control signal.

48. The integrated regulator circuit of claim 47, wherein the memory circuit has at least one storage element for storing the mode of operation of the regulator circuit.

49. The integrated regulator circuit of claim 47, wherein the control circuit further includes a resistor divider network for generating the first reference signal at a first output and the second reference signal at a second output.

50. The integrated regulator circuit of claim 46, wherein the comparator includes:

a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

51. In a power supply, an integrated switching regulator circuit operating in response to a feedback signal from the power supply for providing a switching signal to the power supply, the switching regulator comprising a control input coupled for receiving a mode control signal from external to the integrated switching regulator circuit which suspends the switching signal to the power supply.

52. The integrated switching regulator circuit of claim 51 further including a state control circuit having an input coupled for receiving the mode control signal and an output for providing a mode signal in response to the state control signal to set the mode of operation of the switching regulator circuit.

53. The integrated switching regulator circuit of claim 52, wherein the state control circuit includes a comparator having a first input coupled for receiving the mode control signal, a second input coupled for receiving a first reference signal, and an output for providing the mode signal.

54. The integrated switching regulator circuit of claim 53, wherein the state control circuit further includes a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit as the mode signal according to a value of the control signal.